

Remarks

Claims 1-21 remain in the application. Claims 1, 8, 12, and 18 are hereby amended. No new matter is being added.

Claim Rejections -- 35 U.S.C. 112

Original claims 1 and 12 were rejected under 35 U.S.C. 112, second paragraph, as being incomplete.

Applicants have hereby amended claim 1 so as to recite as follows.

1. A method of compiling a program to be executed on a target central processing unit (CPU), the method comprising: **scheduling user code instructions**; and opportunistically scheduling diagnostic testing of CPU registers so that **testing of the CPU registers occurs within normal running of the user code instructions, and such that if an error in the CPU register is indicated, a jump to a fault handler routine occurs.** (Emphasis added.)

As shown above, applicants have added the step of “**scheduling user code instructions**” (emphasis added) which is a step of compiling the program. Applicants have further added, in relation to the opportunistic scheduling of diagnostic testing of CPU registers, that “**testing of the CPU registers occurs within normal running of the user code instructions, and such that if an error in the CPU registers is indicated, a jump to a fault handler routine occurs.**” (Emphasis added.)

These added claim limitations are supported in the original application, for example, on page 7, lines 19-28 and page 9, lines 7-22, which are reproduced below for convenience of reference.

In accordance with an embodiment of the invention, the scheduling performed **404** includes both the scheduling of user code instructions and the opportunistic scheduling of register diagnostics. In other words, at compile time, the compiler schedules testing of registers so that the testing occurs within the normal running of the user code. The testing may be scheduled opportunistically and intelligently by the compiler to reduce the amount of performance overhead incurred. This scheduling is discussed further below in relation to FIG. 5. This scheduling is performed until a determination **406** is made that the user code is completely scheduled. Thereafter, the scheduling may be considered as completed **408**.

(Page 7, lines 19-28.)

FIG. 7 is a flow chart depicting an example process for diagnostic testing of a register that may be scheduled **508** in accordance with an embodiment of the invention. Note that the process **508** depicted in FIG. 7 is a simple process for explanatory purposes. An actual process as implemented may not have such a simple flow.

Per the process **508** of FIG. 7, known data may be written **702** to the register being tested. As discussed above, the known data may be part of a predetermined **401** test pattern. For instance, the known data may be a checkerboard pattern of zeros and ones. Subsequently, the data may be read **704** from the register being tested.

A comparison **706** may then be made between the data read and the expected data (i.e. the known data). A determination **708** may be made as to whether the compared data is the same. If it is the same, then no error is indicated, and the execution of instructions continues **710**. If it is not the same, then an error in the register is indicated, and a jump **712** to a fault handler may occur.

(Page 9, lines 7-22.)

With the above-discussed amendments, applicants respectfully submit that claim 1 now overcomes this rejection.

Claim 12 is amended similarly as claim 1 is amended. Hence, applicants respectfully submit that claim 12 now also overcomes this rejection for at least the same reasons discussed above in relation to claim 1.

Claim Rejections -- 35 U.S.C. 101

Original claim 12 was rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. In accordance with Examiner's suggestion, applicants have amended claim 12 so as to now recite "A computer-readable medium embedded with a compiler program" Therefore, applicants respectfully submit that amended claim 12 now overcomes this rejection.

Claim Rejections -- 35 U.S.C. 102 (Barto et al)

Original claims 1 and 12 were rejected under 35 U.S.C. 102 as being anticipated by Barto (US 7,127,310). Applicants respectfully traverse this rejection in relation to amended claims 1 and 12.

Applicants have hereby amended claim 1 so as to recite as follows.

1. A method of **compiling a program** to be executed on a target central processing unit (CPU), the method comprising: **scheduling user code instructions; and opportunistically scheduling diagnostic testing of CPU registers so that testing of the CPU registers occurs within normal running of the user code instructions**, and such that if an error in the CPU register is indicated, a jump to a fault handler routine occurs. (Emphasis added.)

As shown above, applicants have amended claim 1 so as to further make clear that the claimed invention is a method of "**compiling a program**" which involves

“scheduling user code instructions” and “opportunistically scheduling diagnostic testing of CPU registers so that testing of the CPU registers occurs within normal running of the user code instructions.” (Emphasis added.)

The function of a compiler is discussed in the original application as follows. “FIG. 2 illustrates example software elements of the illustrative computer system of FIG. 1. Shown are application programs **26**. Such applications **26** may be compiled using a compiler **34** incorporated with the teachings of the present invention. The compiled application programs **26** access the runtime libraries **34** for services during execution, which in turn access the operating system **32** for system services. The compiler **34** also accesses the operating system **32** for system services during compilation of application programs **26**.” (Page 4, lines 21-28.)

In contrast, applicants respectfully submit that the disclosure of Barto et al does not read on the limitations of claim 1. In particular, Barto et al. does not disclose a method for compiling a program. Instead, Barto et al. pertains to a method for **generating a cost function in relation to processing a workpiece**.

For example, **“scheduling opportunistic preventative maintenance or qualifications tests to meet specifications”** (column 7, lines 30-31, emphasis added) referred to in Barto et al does not read on “scheduling user code instructions” and “opportunistically scheduling diagnostic testing of CPU registers so that testing of the CPU registers occurs within normal running of the user code instructions” per the claimed invention.

Therefore, for at least the above-discussed reasons, applicants respectfully submit that claim 1, as amended, now overcomes this rejection.

Claim 12 is amended similarly as claim 1 is amended. Hence, applicants respectfully submit that claim 12 now also overcomes this rejection for at least the same reasons discussed above in relation to claim 1.

Claim Rejections -- 35 U.S.C. 102 (Quach)

Original claims 1-3, 6, 12-14 and 21 were rejected under 35 U.S.C. 102 as being anticipated by Quach (US 6,640,313). Applicants respectfully traverse this rejection in relation to the claims as now amended.

As discussed above, applicants have amended claim 1 so as to further make clear that the claimed invention is a method of **“compiling a program”** which involves **“scheduling user code instructions”** and **“opportunistically scheduling diagnostic testing of CPU registers so that testing of the CPU registers occurs within normal running of the user code instructions.”** (Emphasis added.)

In contrast, applicants respectfully submit that the disclosure of Quach does not read on the limitations of claim 1. In particular, Quach does not disclose a method for compiling a program. Instead, Quach pertains to a **microprocessor** itself. In other words, Quach discloses **hardware circuitry**, while the claimed invention pertains to **compiling a software program** so that it may be subsequently executed on hardware circuitry.

Hence, the **“high reliability (HR) execution mode”** (column 2, lines 39-40, emphasis added) referred to in Quach does not read on “scheduling user code instructions” and “opportunistically scheduling diagnostic testing of CPU registers so that testing of the CPU registers occurs within normal running of the user code instructions” per the claimed invention.

Therefore, for at least the above-discussed reasons, applicants respectfully submit that claim 1, as amended, now overcomes this rejection.

Claims 2-3 and 6 depend from claim 1. Hence, applicants respectfully submit that claims 2-3 and 6 now also overcomes this rejection for at least the same reasons discussed above in relation to claim 1.

Claim 12 is amended similarly as claim 1 is amended. Hence, applicants respectfully submit that claim 12 now also overcomes this rejection for at least the same reasons discussed above in relation to claim 1.

Claims 13-14 and 21 depend from claim 12. Hence, applicants respectfully submit that claims 13-14 and 21 now also overcome this rejection for at least the same reasons discussed above in relation to claim 12.

Claim Rejections -- 35 U.S.C. 103 (Quach in view of Raina)

Original claims 7-10 and 17-20 were rejected under 35 U.S.C. 103 as being unpatentable over Quach as applied to claim 1 above in view of Raina (US 6,134,675). Applicants respectfully traverse this rejection in relation to the claims as now amended.

As discussed above, applicants respectfully submit that amended claims 1 and 12 are now patentably distinct over Quach.

Claims 7-10 depend from claim 1, and claims 17-20 depend from claim 12. Hence, applicants respectfully submit that claims 7-10 and 17-20 now also overcome this rejection for at least the same reasons discussed above in relation to claim 1 and 12, respectively.

In addition, applicants respectfully note that, like Quach, Raina discloses **hardware circuitry**, while the claimed invention pertains to **compiling a software program** so that it may be subsequently executed on hardware circuitry.

Claim Rejections -- 35 U.S.C. 103 (Barto et al in view of Schreiber)

Original claim 11 was rejected under 35 U.S.C. 103 as being unpatentable over Barto et al in view of Schreiber 6,460,173). Applicants respectfully traverse this rejection in relation to the claims as now amended.

Original claim 11 recites as follows.

11. A method of **compiling a program** to be executed on a target central processing unit (CPU), the method comprising:
 opportunistically scheduling diagnostic testing of CPU registers;

checking a predetermined level of aggressiveness for the scheduling of
the register diagnostic testing;
determining a next register to be tested;
determining if there is sufficient opportunity to schedule a register
diagnostic instruction to test the next register;
if there is sufficient opportunity, then **scheduling the register diagnostic
instruction to test the next register**; and
if there is insufficient opportunity, then **scheduling user code
instructions**.

(Emphasis added.)

As shown above, original claim 11 makes clear that the claimed invention is a method of **“compiling a program”** which involves, for example, **“scheduling the register diagnostic instructions to test the next register”** and **“scheduling user code instructions.”** (Emphasis added.)

In contrast, applicants respectfully submit that the disclosure of Barto et al does not read on the limitations of claim 11. In particular, Barto et al. does not disclose a method for compiling a program. Instead, Barto et al. pertains to a method for **generating a cost function in relation to processing a workpiece**.

For example, **“scheduling opportunistic preventative maintenance or qualifications tests to meet specifications”** (column 7, lines 30-31, emphasis added) referred to in Barto et al does not read on “scheduling the register diagnostic instructions to test the next register” and “scheduling user code instructions.”

Furthermore, applicants respectfully submit that Schreiber discloses **hardware circuitry**, while the claimed invention pertains to **compiling a software program** so that it may be subsequently executed on hardware circuitry. For example, as described in Schreiber, “These inventions relate to processor design, and more specifically to allocation of function units in processor design” (Column 1, lines 21-24.)

Therefore, for at least the above-discussed reasons, applicants respectfully submit that claim 11 is patentable over Barto et al in view of Schreiber.

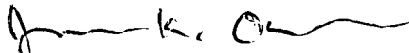
Conclusion

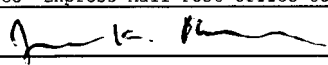
For the above-discussed reasons, applicant believes that the pending claims, as amended, now overcome all the rejections of the office action. Favorable action is respectfully requested.

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 08-2025 (Hewlett Packard).

Respectfully Submitted,

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